

Raymond C. Jimenez

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- EDUCATION ◇ **California Institute of Technology**, Pasadena, CA *June 2013*
BS, Electrical Engineering GPA: 3.7
Course Emphasis: Digital Logic Design and System Integration
- WORK ◇ **Hardware Development Electrical Engineer**, SpaceX *July 2013–present*
EXPERIENCE ◇ **Teaching Assistant**, Senior EE Project Course, Caltech *Oct 2012–June 2013*
Instructor: Barry Megdal, Lecturer in Electrical Engineering
- Aided students in troubleshooting analog designs (e.g., Wien bridge oscillators, quadrature oscillators, basic power supplies)
 - Provided general design/project advice
- ◇ **Research Intern**, Mitsubishi Electric, Ofuna, Japan *Jun 2012–Sept 2012*
Mentor: Masaki Hamada, Information Display Group
- Designed and implemented an efficient FPGA radial gradient algorithm, using one-tenth the expected resources in one-fifth the time
 - Researched embedded image stitching algorithms, resulting in an unoptimized implementation
- ◇ **Research Intern**, Scherer Nanofabrication Group, Caltech *Jun 2010–Dec 2012*
Caltech Summer Undergraduate Research Fellowship (SURF)
Mentor: Axel Scherer, Bernard A. Neches Professor of Electrical Engineering, Applied Physics, and Physics
- Designed several ASIC CMOS neural probes using Cadence EDA tools
 - Optimized circuits for super-low power usage (100s of μW)
 - Designed ring oscillators and VCOs, optimizing for space and simplicity
- Projects:
- *Super-small, Wireless CMOS Neural Probes*
- ◇ **Senior Sysadmin**, Dabney House, Caltech *Feb 2010–June 2013*
- Created a real-time transcoding and video streaming interface to access large amounts of house multimedia
 - Developed a large-scale (100+ TiB), highly-expandable, reliable storage system using commodity hardware and software
 - Developed a simple, **sh**-based search engine for local file systems
- ◇ **Research Intern**, Marsden CDS Group, Caltech *Jun 2009–Aug 2009*
Caltech Freshman Summer Research Institute (FSRI)
Mentor: Jerrold Marsden, Carl F. Braun Professor of Engineering
- Implemented fluid-metric computation software for GPUs using NVidia's CUDA
 - Obtained efficient algorithms for calculating LCS fields for given streamfunctions, with speedups of up to 1000 \times owing to parallelization
 - Software, papers, and analysis available at
<http://www.its.caltech.edu/~raymondj/LCS/>

- WORK EXPERIENCE (CONTINUED)
- ◇ **Laboratory Intern**, Bellan Plasma Group, Caltech *Jun 2007–Jun 2009*
 Mentor: Paul Bellan, Professor of Applied Physics
 - Worked to produce high-intensity pulsed magnetic fields using PCB coils
 - Constructed several vacuum devices for testing
 - Verified that fields of up to 3T for 100ns are possible using commodity hardware
 - ◇ **System Architect**, Vignettes for Training, Duarte, CA *Dec 2007–Sep 2008*
 - Created a e-Learning social networking application (TrainingPayback, sample site available at <http://www.trainingmagnetnetwork.com>)
 - Implemented the first revision with Ruby on Rails
 - Maintained system during its first year, where it expanded to over 20,000 users; handled day-to-day maintenance and bug fixes
- HONORS AND AWARDS
- ◇ **Caltech Japan Internship Fellow** *2012*
 - ◇ **Rose Hills Foundation SURF Fellow** *2011*
 - ◇ **Caltech SURF Fellow** *2010*
 - ◇ **Caltech FSRI Fellow** *2009*
- SELECTED INDEPENDENT PROJECTS
- ◇ **FPGA-based FLAC decoder/player** *January 2012–January 2013*
 - Developed a fully-integrated hardware FLAC decoding core, embedded AVR core, and peripherals (UART, SD card, DMA), resulting in a stand-alone FLAC player
 - Realized a homebrew 2nd-order 1024x oversampling sigma-delta DAC with 0.1% THD+N
 - ◇ **Electrostatic Headphone Amplifier** *March 2012–October 2012*
 - Prototyped an original design for high-voltage ($\pm 400\text{V}$) audio systems
 - First design known to apply high-gain global feedback, cancelling component variance
 - Low distortion ($< 0.05\%$) and high frequency response (0-1MHz, $\pm 2\text{dB}$)
 - ◇ **Amateur Synchrotron Accelerator (ASA)** *2008–Present*
 - Currently conducting feasibility studies of a small (4m) amateur synchrotron, capable of producing 10MeV electrons.
 - ◇ **Nuclear Fusion (Farnsworth Fusor)** *June 2006–June 2008*
 - Successfully built a device for performing deuterium-deuterium fusion, including vacuum system and high voltage equipment
 - Published a book, *Amateur Nuclear Fusion*, ISBN: 978-0-9791847-2-7, available via Lulu, which documents my experience
- SKILLS
- ◇ **Electronics**: Familiar with advanced (digital and analog) circuit design, from ASIC-level implementation to large-scale system design.
 - ◇ **High Voltage**: Familiar with construction of $\geq \pm 35\text{kV}$ transformer-based supplies
 - ◇ **High Vacuum**: Familiar with design/operation of systems at $\leq 5.0 \times 10^{-4}$ Torr
 - ◇ **Computer Networking**: Proficient with BGP, OSPF, RIP, IPv6, Zebra/Quagga; familiar with dynamic routing in general
 - ◇ **Operating Systems**: Linux/FreeBSD system administration
 - ◇ **Computer Languages**: Proficient in VHDL, C, Haskell; familiar with \LaTeX , Javascript (node.js, jQuery), bash, regexes
 - ◇ **Miscellaneous**: Scientific glassblowing, intermediate spoken Japanese, unicycling